

;PALASM Design Description

;----- Declaration Segment -----

TITLE GLUE21 - Glue Logic for 68000 Microprocessor
 PATTERN U28 of Control Module
 REVISION 2.1
 AUTHOR Alen Koebel
 COMPANY ELECTROHOME LTD.
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CHIP GLUE PALCE22V10

;----- Description Segment -----

; The GLUE pal provides several functions for the 68000 system that
 ; serve to "glue" it together:
 ;
 ; - chip select generation (active low) for the program EPROM,
 ; the battery-backed RAM chips, the SPARE slot, the external bus
 ; buffers, the convergence circuit and the character generator.
 ;
 ; - data-transfer-acknowledge (DTACK) generation (active low) for
 ; the 68000. All data transfers are zero wait state except those
 ; involving the character generator. Read or write access to the
 ; character generator during a video scan will result in the
 ; insertion of wait states until a horizontal or vertical blanking
 ; interval occurs. This prevents glitching of the screen.
 ;
 ; - interrupt acknowledge signal (IACK) generation (active low)
 ; for inputting to the VPA pin of the 68000 in response to
 ; interrupts captured by U29. This enables autovectoring.

; Revision History

; 1.X - all 1.X versions were based on a 16V8 device
 ; 2.0 - first version for 22V10
 ; 2.1 - deleted wait state insertion for convergence circuit
 ; (did not work - needs additional delays)

;----- PIN Declarations -----

PIN 1	8M	COMBINATORIAL ; INPUT	8 MHz clock
PIN 2	CBLANK	COMBINATORIAL ; INPUT	composite blanking signal
PIN 3	CS_CHARI	COMBINATORIAL ; INPUT	"raw" char gen chip select
PIN 4	AS	COMBINATORIAL ; INPUT	68k address strobe
PIN 5	FC0	COMBINATORIAL ; INPUT	68k function code bit0
PIN 6	FC1	COMBINATORIAL ; INPUT	68k function code bit1
PIN 7	FC2	COMBINATORIAL ; INPUT	68k function code bit2
PIN 8	CS_WAVEI	COMBINATORIAL ; INPUT	"raw" conv. chip select
PIN 9	A16	COMBINATORIAL ; INPUT	68k address bit
PIN 10	A17	COMBINATORIAL ; INPUT	68k address bit
PIN 11	A18	COMBINATORIAL ; INPUT	68k address bit
PIN 12	GND		
PIN 13	A19	COMBINATORIAL ; INPUT	68k address bit
PIN 14	DTACKDLY	REGISTERED ; OUTPUT	delayed DTACK
PIN 15	DTACK	COMBINATORIAL ; OUTPUT	data transfer acknowledge
PIN 16	IACK	COMBINATORIAL ; OUTPUT	interrupt acknowledge
PIN 17	CS_ROM	COMBINATORIAL ; OUTPUT	EPROM chip select (U35)
PIN 18	CS_RAM	COMBINATORIAL ; OUTPUT	RAM chip select (U31,U32)
PIN 19	CS_EXT	COMBINATORIAL ; OUTPUT	external bus buffer select
PIN 20	CS_SPARE	COMBINATORIAL ; OUTPUT	SPARE slot select
PIN 21	CS_WAVE	COMBINATORIAL ; OUTPUT	convergence chip select